AMENDMENTS TO THE CLAIMS

The claims and their status are reflected below. Claims 1-5, 8-18, 20-31 and 33-36 are pending in the application.

1. (previously presented) A flash memory device formed from a substrate, the device comprising:

strings of transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate,

each floating gate having at least two sides perpendicular to the axes of the strings;

a conductive isolating member adjacent to each of the at least two perpendicular sides of the floating gate and located between adjacent transistors in the strings of transistors, each isolating member shielding a selected floating gate from a charge stored in an adjacent component;

wherein the isolating members and the wordlines comprise a conductive material;

wherein the isolating members are electrically connected to a wordline above a floating gate that the isolating members shield;

wherein the floating gates are approximately T shaped; and

wherein isolating members electrically coupled to the wordlines flank the floating gates.

2. (original) The flash memory device of claim 1, wherein the floating gates are formed between shallow trench isolation areas and wherein the device further comprises wordlines extending across adjacent strings and extending between the floating gates into the shallow trench isolation areas thereby isolating adjacent floating gates.

3. (original) The flash memory device of claim 1 wherein the isolating members have two principal faces, the faces substantially parallel to the at least two sides of each floating gate and substantially perpendicular to the axes of the strings.

4. (original) The flash memory device of claim 1 wherein the isolating members extend a distance between the substrate and an upper level of the floating gates.

5. (original) The flash memory device of claim 4 wherein the floating gates have an upper level and a lower level, the isolating members extending from the substrate a distance between the lower and upper level.

6-7. (canceled)

8. (original) The flash memory device of claim 1 wherein the isolating members shield a floating gate of the plurality of floating gates from an electrical field of an adjacent floating gate, thereby minimizing field effect coupling between adjacent floating gates.

9. (original) The flash memory device of claim 8 wherein the adjacent floating gate is diagonally adjacent or horizontally adjacent to the selected floating gate and wherein the isolating members further minimize field effect coupling in the wordline direction.

10. (previously amended) A non-volatile memory device comprising:

floating gates that store a charge;

bitlines that select amongst the floating gates, each bitline having a bitline axis;

wordlines that select amongst the floating gates;

conductive sidewall elements positioned along the bitline axes, the sidewall elements located at sides of the floating gates between adjacent floating gates, the sidewall elements shielding the floating gates; and

wherein the non-volatile storage device is NAND flash memory.

11. (original) The memory device of claim 10 wherein the sidewall elements shield the floating gates from an electrical field having a component in the direction of the bitline axes.

12. (original) The memory device of claim 10 wherein the sidewall elements extend from the substrate to the floating gates.

13. (original) The memory device of claim 12 wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the lowermost surface.

14. (original) The memory device of claim 12 wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the uppermost surface.

15. (previously amended) The memory device of claim 10 wherein the sidewall elements are electrically coupled to a wordline located between adjacent pairs of sidewall elements.

16. (original) The memory device of claim 15 wherein the coupled sidewalls effectively increase the surface area of the wordline and the electrical coupling between the wordline and the floating gates, thereby aiding in read and write operations.

17. (previously amended) The memory device of claim 10 wherein the wordlines extend between adjacent floating gates so as to shield a selected floating gate from an electrical field of adjacent floating gates.

18. (previously amended) A method of forming NAND flash memory comprising:

forming a plurality of NAND strings of floating gates;

forming control gates above the floating gates;

forming bitlines, the bitlines used together with the control gates to read and write from a floating gate,

the direction of the bitlines substantially perpendicular to the direction of the control gates, the floating gates having bitline sides in the bitline direction and control gate sides in the control gate direction;

forming conductive members between the bitline sides of the floating gates, the members shielding the floating gates from electrical fields having a component in the bitline direction.

19. (canceled)

20. (previously amended) A flash memory device comprising:

floating gates for storing data located above a substrate;

means for isolating adjacent floating gates in the wordline direction;

means for isolating adjacent floating gates in the bitline direction;

means for reading the data stored in the floating gates, the means for reading the data located above the floating gates and interconnecting strings of floating gates, the means for isolating adjacent floating gates in the bitline direction electrically connected to the means for reading the data;

wherein the means for reading the floating gates extends within the means for isolating adjacent floating gates in the wordline direction.

21. (original) The flash memory device of claim 20 wherein the means for reading shields adjacent floating gates from Yupin effect errors and from disturbs.

22. (original) A method of making a memory device in a substrate comprising:

forming a series of floating gates between a first set of trenches each floating gate having two approximately parallel bitline sides and two approximately parallel roughly rectangular wordline sides;

forming a second set of parallel trenches in an oxide layer deposited within the first set of trenches;

forming a wordline above adjacent floating gates, the wordline extending into the second set of trenches and isolating one of the floating gates from a charge applied at an adjacent floating gate; and

forming a conductive element at each of the approximately parallel bitline sides of the floating gates.

23. (original) The method of claim 22 wherein the conductive elements are located on both sides of a floating gate and wherein the method further comprises electrically contacting the elements to the wordline that selects the floating gate.

24. (original) The method of claim 23 wherein the conductive elements shield a selected floating gate from an electrical field of an adjacent floating gate and minimize field effect coupling in the bitline direction between adjacent floating gates.

25. (original) The method of claim 24 wherein the adjacent floating gate is diagonally adjacent or horizontally adjacent to the selected floating gate and wherein the conductive elements further minimize field effect coupling in the wordline direction.

26. (original) The method of claim 22 wherein the memory device formed is a NAND flash memory device.

27. (currently amended) A method of making a non-volatile memory array, comprising:

forming a plurality of NAND strings of flash memory cells, memory cells having floating gates extending across the surface of a substrate and forming a plurality of control gates extending in a first direction and overlying the plurality of strings of floating gates, the plurality of strings of floating gates extending in a second direction that is perpendicular to the first direction;

forming insulating elements along sides of the plurality of floating gates that extend in the first direction, the insulating elements extending above lower surfaces of the plurality of control gates; and

forming conductive sidewall portions overlying insulating elements, the conductive portions in contact with control gates but insulated from floating gates by the insulating elements.

28. (previously presented) The method of claim 27 wherein the insulating elements are first formed to extend along the sides of the plurality of floating gates and along sides of the plurality of control gates and are subsequently etched to provide a contact area to the control gates.

29. (previously presented) The method of claim 27 further comprising, subsequent to the forming the conductive sidewall portions, implanting source and drain regions.

30. (previously presented) The method of claim 29 further comprising forming protective spacers on sides of the conductive sidewall portions and wherein the implanting is in a region defined by the protective spacers.

31. (previously amended) A non-volatile memory array, comprising:

a plurality of floating gates on a substrate;

a plurality of control gates, an individual control gate overlying a floating gate of the plurality of floating gates so that first and second sides of the control gate are coplanar with first and second sides of the floating gate;

a first insulating element covering the first side of the floating gate and extending to partially cover the first side of the control gate;

a second insulating element covering the second side of the floating gate and extending to partially cover the second side of the control gate;

a first conductive sidewall that extends from the first side of the control gate and overlies the first insulating element;

a second conductive sidewall that extends from the second side of the control gate and overlies the second insulating element; and

wherein the floating gate is T-shaped in cross-section.

32. (canceled).

33. (previously amended) The non-volatile memory array of claim 31 wherein the T-shaped floating gate extends over first and second shallow-trench isolation areas.

34. (previously presented) The non-volatile memory array of claim 33 wherein both first and second shallow-trench isolation areas have trenches in their upper surfaces and a wordline extends into the trenches, the wordline connected to the control gate.

35. (previously added) The non-volatile memory device of claim 10 wherein the sidewall elements are not electrically connected to a wordline.

36. (previously added) The method of claim 18 wherein the conductive members are not electrically connected to the control gates.